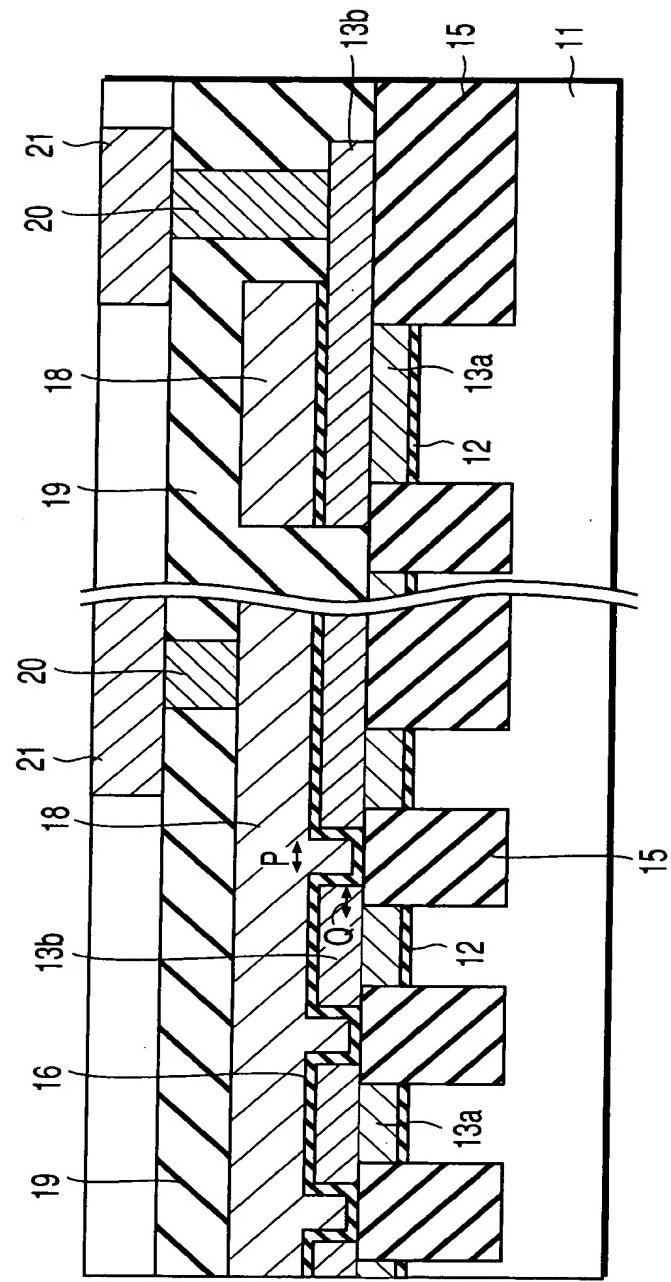


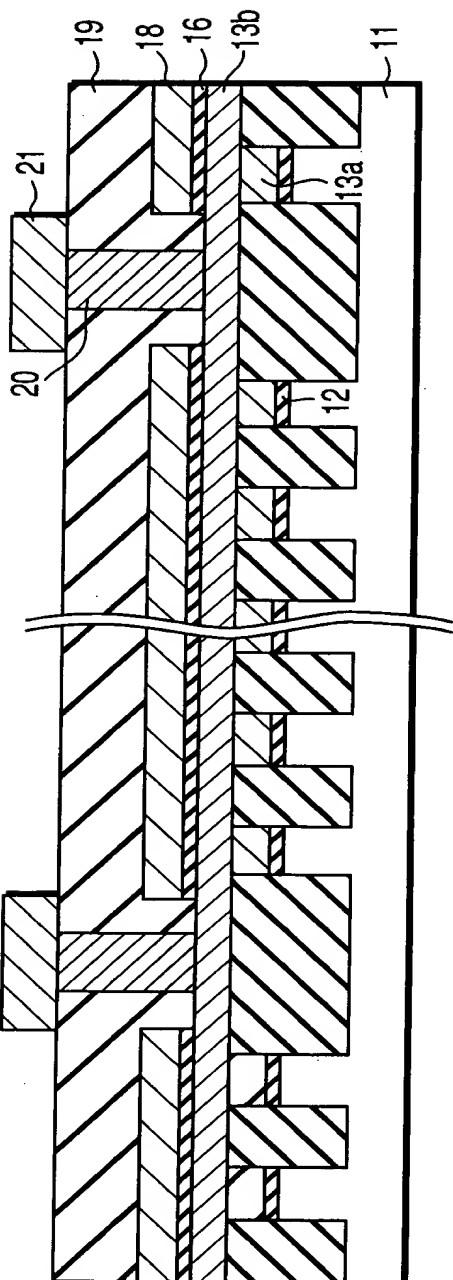
FIG. 46A
Related Art

FIG. 46B
Related Art



Memory cell array region Peripheral circuit region

FIG. 47A Related Art



Selective gate region

FIG. 47B
Related Art

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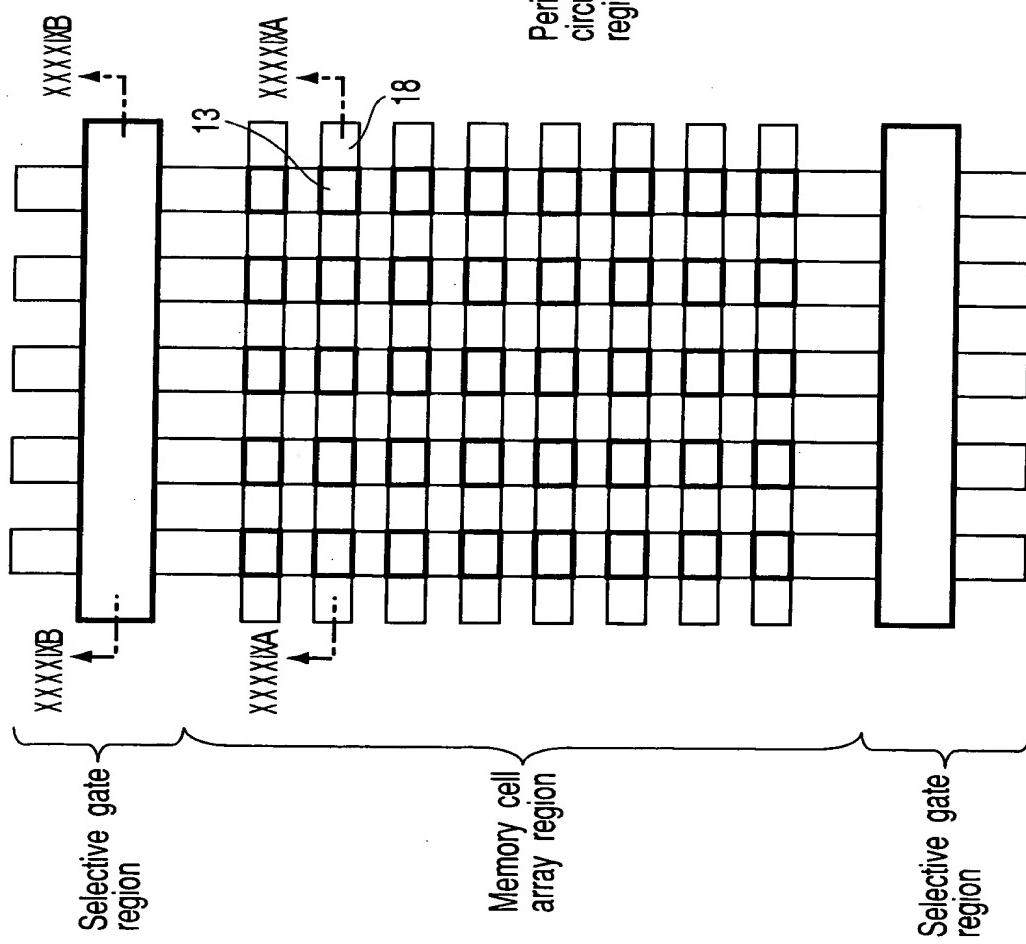


FIG. 48A
Related Art

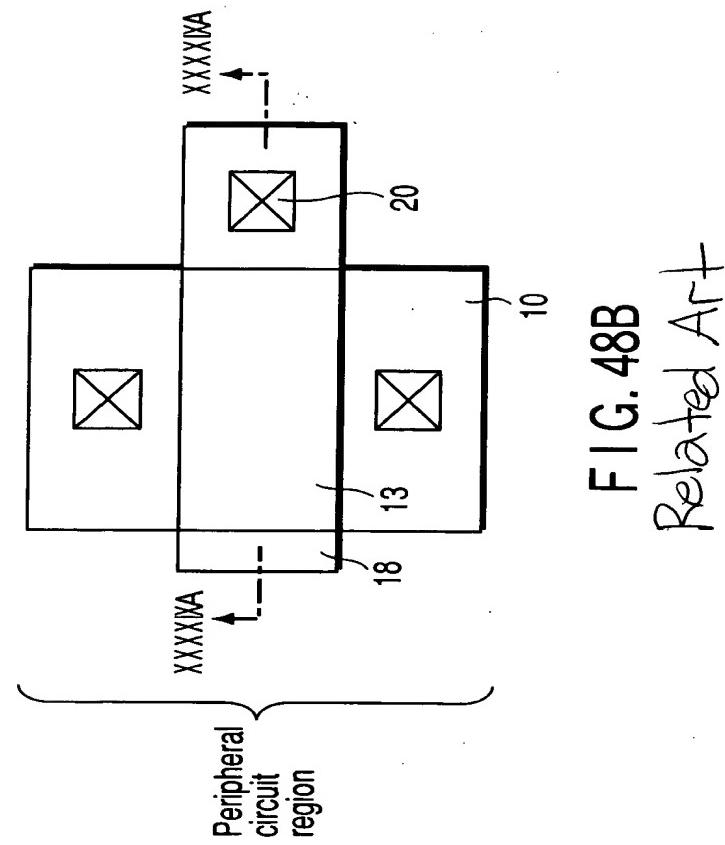
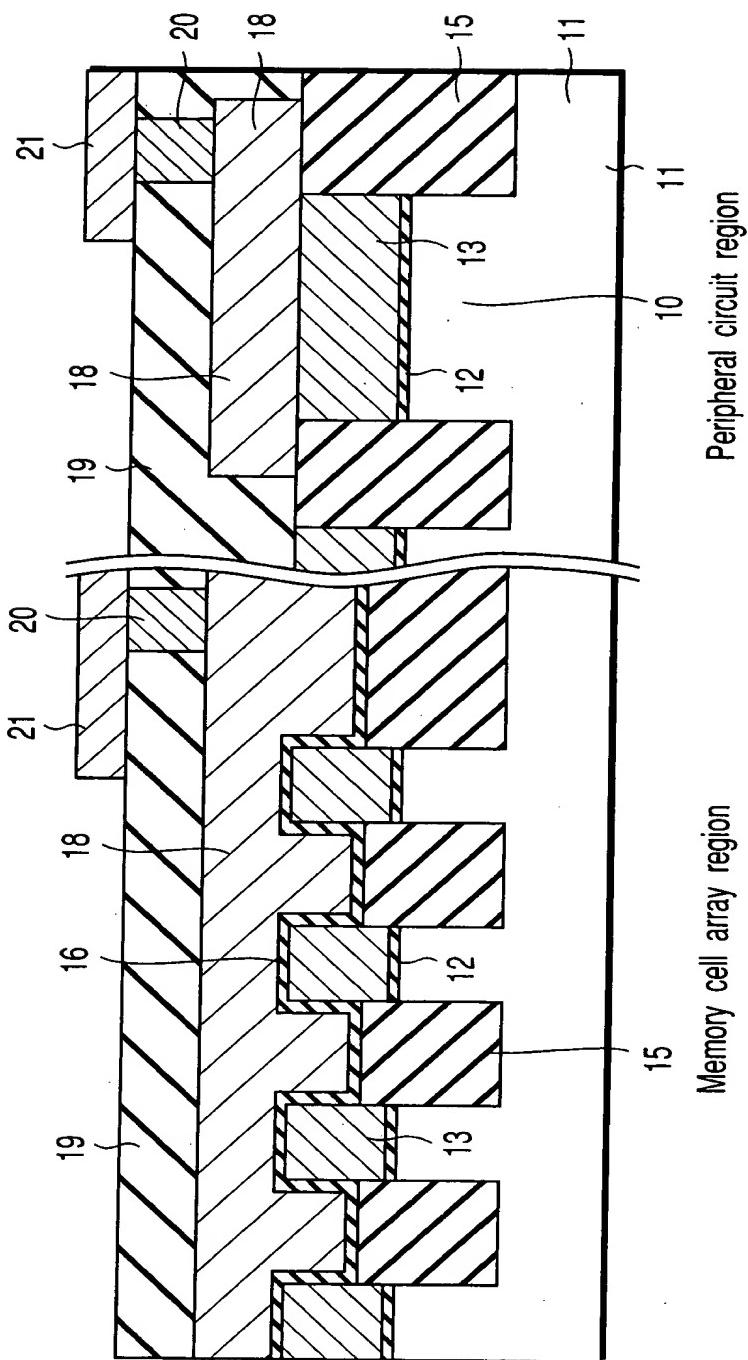


FIG. 48B
Related Art

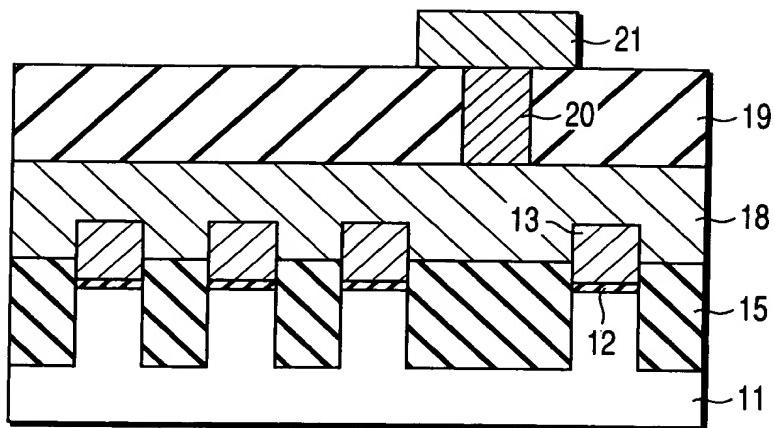
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Memory cell array region

Peripheral circuit region

FIG. 49A
Related Art



Selective gate region

FIG. 49B
Related Art